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Attorney's Do. No. 5038-62
Client Ref. No. P9612

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Enclosed for filing is a patent application under 37 CFR 1.53(b) of:

Inventor(s): John B. Halbert and Randy M. Bonella

For: MEMORY MODULE HAVING BUFFER FOR ISOLATING STACKED MEMORY DEVICES

Enclosures:
- ☒ Specification (pages 1-3); claims (pages 4-6); abstract (page 7)
- ☒ 3 sheet(s) of INFORMAL drawings
- ☒ Declaration or Combined Declaration and Power of Attorney (unsigned)
- ☒ Return Postcard

CLAIMS AS FILED

For	Number Filed	Number Extra	Rate	Basic Fee $ 690
Total Claims	23-20	3	x $ 18 =	$ 54
Independent Claims	3-3	0	x $ 78 =	$ 0
TOTAL FILING FEE				$ 744

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Docket No. 5038-62
Client Ref. No. P9612

PATENT

UNITED STATES APPLICATION FOR LETTERS PATENT

for

MEMORY MODULE HAVING BUFFER FOR ISOLATING STACKED MEMORY DEVICES

By

John B. Halbert and Randy M. Bonella

Filed

September 18, 2000

MEMORY MODULE HAVING BUFFER FOR ISOLATING STACKED MEMORY DEVICES

BACKGROUND OF THE INVENTION

Fig. 1 is a block diagram of a prior art memory system. The system of Fig. 1 includes three memory modules 10, 12, and 14 that are coupled to a memory controller 16 through a bus 18. Each memory module is fabricated on a circuit board that plugs into a connector 20 on a mother board 22. Each module includes multiple memory devices 24, 26, and 28 that are coupled to the bus 18 to allow the memory controller to access the memory devices.

To increase the memory density of the modules, memory devices can be stacked on top of each other, thereby increasing the memory capacity of each module without increasing the space required on the circuit board. Stacking memory devices, however, increases the capacitive loading of the signals on the bus. For example, from the perspective of the memory controller 16, each data line in the bus 18 has a total capacitance that equals the sum of the capacitance of each portion of the signal line running through sections A, B, and C of the bus, plus the capacitance of the portion of the data line in sections 30, 32, and 34 that couple the memory devices to the bus, plus the sum of the input capacitance of all of the memory devices (which are attached to sections 30, 32, and 34 in parallel). If additional memory devices are stacked on devices 24, 26, and 28, then the capacitance of the additional devices are added to the total capacitance seen by the controller. Therefore, when the memory controller drives a data signal onto the bus, it must overcome the combined capacitance of all of the stacked memory devices. This heavy capacitive loading reduces the maximum operating speed and increases the power consumption by the memory system, especially at higher operating frequencies.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a prior art memory system.

Fig. 2 is a block diagram of an embodiment of a memory module in accordance with the present invention.

Fig. 3 is a side view showing the mechanical arrangement of an embodiment of a memory module in accordance with the present invention.

Fig. 4 is a block diagram of an embodiment of a memory system in accordance with the present invention.

DETAILED DESCRIPTION

Fig. 2 is a block diagram of an embodiment of a memory module 100 in accordance with the present invention. Module 100 includes a first memory device 104 which is mounted on a circuit board 108. A second memory device 106 is stacked on top of the first memory device to form a stack 102. A buffer 110 is mounted on the circuit board and electrically coupled to the memory devices 104 and 106 through signal lines 112. A connector 114 is attached to the circuit board for coupling the memory module to a bus that leads to a memory controller on another circuit board, e.g., a computer mother board. The buffer 110 is arranged to capacitively isolate the stack of memory devices from the bus. Therefore, the capacitive loading seen by a memory controller (or other device) driving the bus is reduced. This increases the maximum operating speed of the memory module and reduces power consumption.

The buffer 110 sends and receives signals to and from the memory controller through connector 114 over signal lines 120. In a preferred embodiment, the buffer 110 is designed to receive signals from the memory controller over a first bus and redrive them back out the connector over signal lines 122 (shown in broken lines) and to a second memory module over a second bus.

Fig. 3 is a side view showing the mechanical arrangement of an embodiment of a memory module in accordance with the present invention. The stack 102 can be extended to include additional memory devices (shown in broken lines). Additional stacks can also be added, and they can be buffered by the first buffer 110, or a separate buffer can be used for each stack.

Fig. 4 is a block diagram of an embodiment of a memory system in accordance with the present invention. The system of Fig. 4 includes two modules 100A and 100B coupled to a memory controller 116 on a computer mother board 117 through a bus system 118 which includes buses 118A and 118B. The modules may be coupled through connectors 130A and 130B which plug into connectors 132A and 132B, respectively, on the mother board. Each

module a stack of memory devices 102A,102B and a buffer 110A,110B that isolates the corresponding stack from the bus system. In the example of Fig. 4, the modules are coupled to the memory controller in a point-to-point arrangement. That is, the memory controller 116 is coupled to module 100A, which is designed to receive signals from the memory controller and redrive them to module 100B. The use of point-to-point wiring further reduces the capacitive loading seen by the memory controller. Alternatively, the modules 110A and 110B and memory controller 116 may be coupled together in a multi-drop arrangement in which both of the modules are essentially coupled in parallel on a single bus.

The memory controller 116 is shown in Fig. 4 as part of a central processing unit (CPU) 126, however, it may alternatively be implemented as one chip of a chipset, or in any other suitable form. The memory system shown in Fig. 4 includes two memory modules for purposes of illustration, but may be implemented with only a single memory module or with any number of modules. The buffers need not be mounted on the memory modules, but can also be mounted on the mother board or any other device on which the bus system resides. Moreover, the stacks of memory devices need not be mounted on modules. Instead, an entire memory system in accordance with the present invention may be fabricated on a single circuit board including the memory controller, bus, stacks of memory devices, and buffers arranged to capacitively isolate the stacks from the bus. The advantages of the present invention can be realized wherever memory devices are stacked by buffering the stack from other components, thereby reducing the capacitance load seen by the other component.

Having described and illustrated the principles of the invention in some preferred embodiments thereof, it should be apparent that the invention can be modified in arrangement and detail without departing from such principles. We claim all modifications and variations coming within the spirit and scope of the following claims.

CLAIMS

1. A memory system comprising:

a first memory device;

a second memory device stacked on the first memory device; and

a buffer coupled to the first and second memory devices.

2. A memory system according to claim 1 further comprising a third memory device stacked on the second memory device and coupled to the buffer.

3. A memory system according to claim 1 further comprising a bus coupled to the buffer.

4. A memory system according to claim 3 further comprising a memory controller coupled to the bus.

5. A memory system according to claim 1 wherein the buffer is a first buffer and further comprising:

a third memory device;

a fourth memory device stacked on the third memory device; and

a second buffer coupled to the third and fourth memory devices and to the first buffer.

6. A memory system according to claim 5 wherein the first buffer is adapted to receive a signal and redrive the signal to the second buffer.

7. A memory system according to claim 5 wherein the first buffer is adapted to receive a plurality of signals and redrive the plurality of signals to the second buffer.

8. A memory system according to claim 5 further comprising a memory controller coupled to the first buffer.

9. A memory system according to claim 8 wherein the memory controller, the first buffer, and the second buffer are coupled together in a multi-drop arrangement.

10. A memory system according to claim 8 wherein the memory controller, the first buffer, and the second buffer are coupled together in a point-to-point arrangement.

11. A memory module comprising:

a first memory device;

a second memory device stacked on the first memory device; and

a buffer coupled to the first and second memory devices and arranged to capacitively isolate the first and second memory devices from a bus.

12. A memory module according to claim 11 further comprising a connector attached to the module and adapted to couple the module to a bus.

13. A memory module according to claim 11 further comprising a third memory device stacked on the second memory device and coupled to the buffer.

14. A memory module according to claim 11 wherein the memory module is adapted to receive a signal from the bus and to redrive the signal to another memory module.

15. A memory module according to claim 11 wherein the memory module is adapted to receive a plurality of signals from the bus and to redrive the plurality of signals to another memory module.

16. A memory module according to claim 11 wherein the buffer is adapted to receive a signal from the bus and to redrive the signal to another memory module.

17. A memory system comprising:

a bus;

a stack of memory devices; and

a buffer coupled between the stack of memory devices and the memory bus.

18. A memory system according to claim 17 further comprising:

a second stack of memory devices; and

a second buffer coupled between the second stack of memory devices and the bus.

19. A memory system according to claim 17 wherein the buffer is a first buffer and further comprising:

a second stack of memory devices; and

a second buffer coupled between the second stack of memory devices and the first buffer.

20. A memory system according to claim 17 further including a memory controller coupled to the bus.

21. A memory system according to claim 17 wherein the stack of memory devices is mounted on a memory module.

22. A memory system according to claim 21 wherein the buffer is mounted on the memory module.

23. A memory system according to claim 21 wherein the bus is fabricated on a circuit board and the buffer is mounted on the circuit board.

ABSTRACT

The present invention utilizes a buffer to isolate a stack of memory devices, thereby taking advantage of the increased memory density available from stacked memory devices while reducing capacitive loading. A memory module in accordance with the present invention may include a stack of memory devices and a buffer coupled to the first and second memory devices and arranged to capacitively isolate the first and second memory devices from a bus. In a memory system in accordance with the present invention, multiple buffered stacks of memory devices are preferably coupled in a point-to-point arrangement, thereby further reducing capacitive loading.

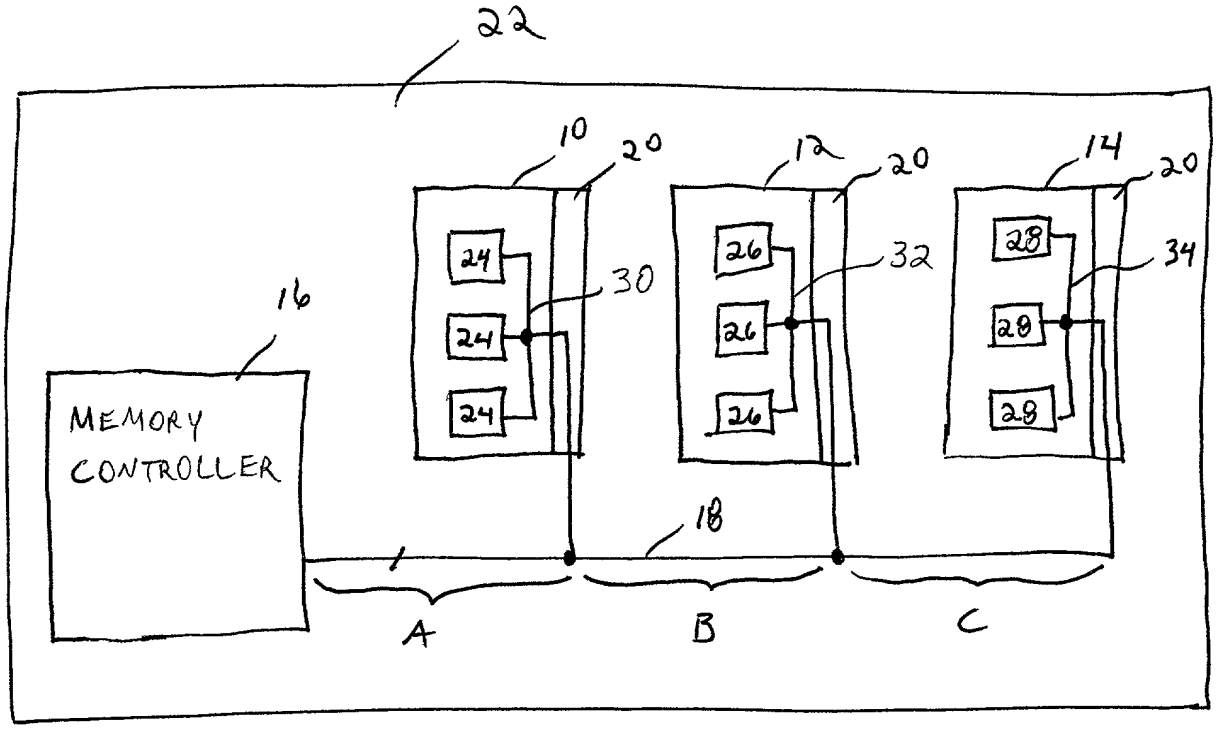

Fig. 1 (PRIOR ART)

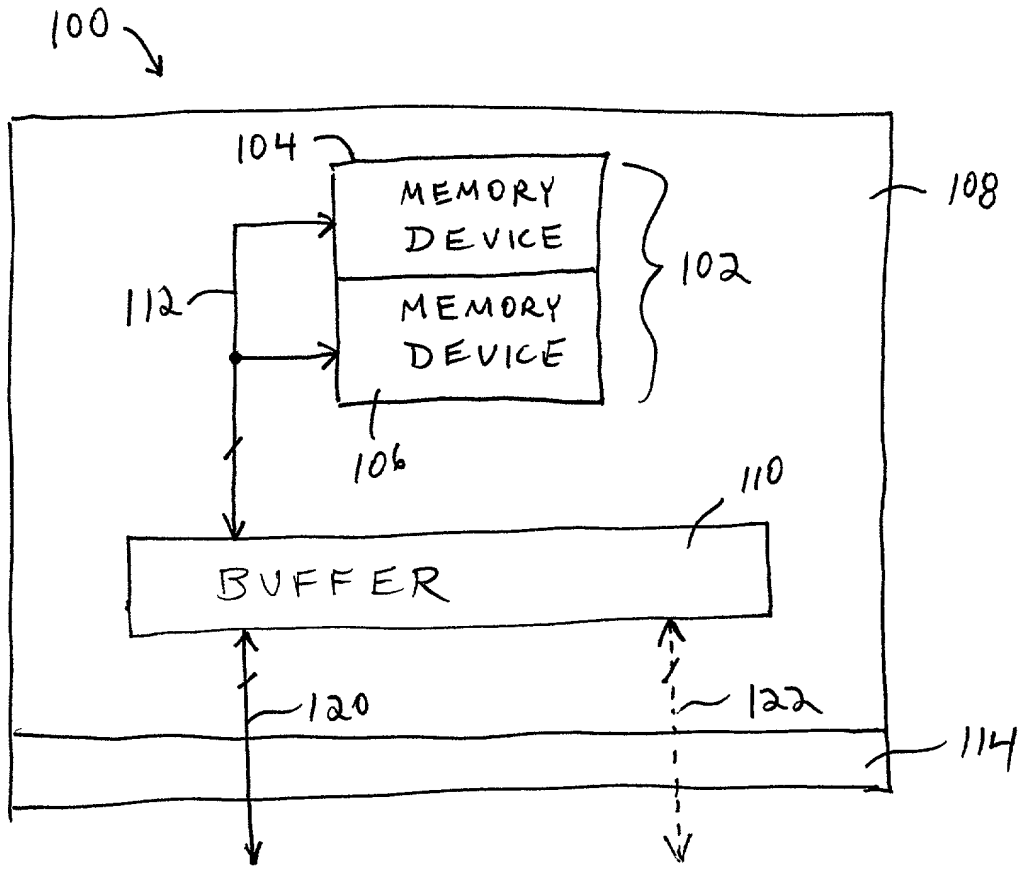

Fig. 2

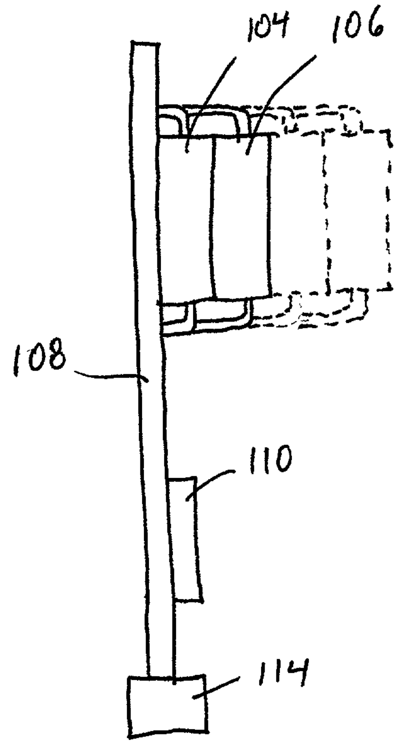

Fig. 3

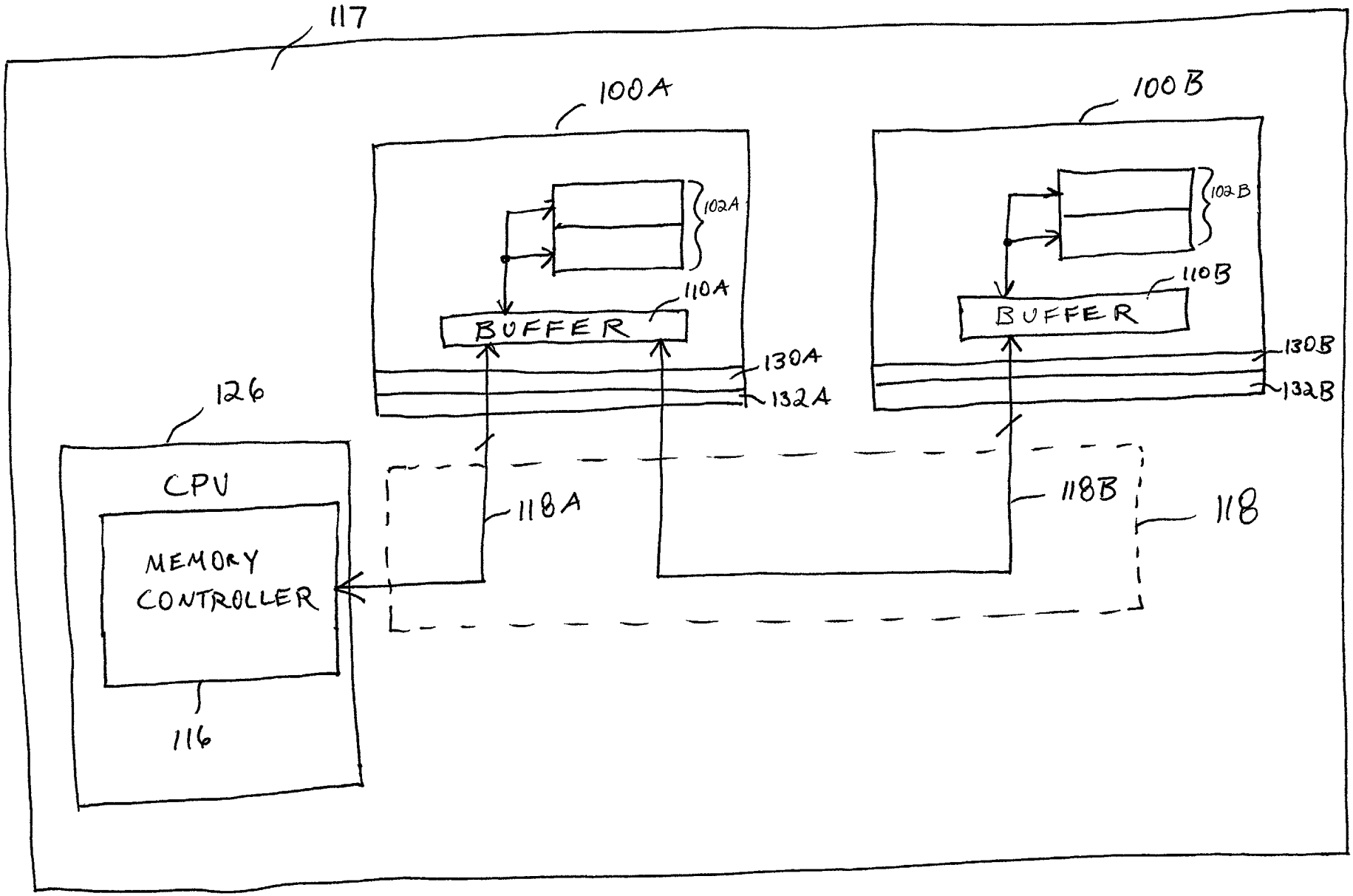

Fig. 4

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[X] is attached hereto.
[ ] was filed on _____ as Application No. _____
[ ] and was amended on _____(if applicable)
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I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

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I hereby claim foreign priority benefits under Title 35, United States Code, Sec. 119 (a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Claiming Priority?	
_____	_____	_____	[ ]	[ ]
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Sec. 119(e) of any United States provisional application listed below:

Provisional Application No.	Filing Date
_____	_____

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(Application No.)	(Filing Date)	(Status) (patented, pending, abandoned)

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